AF # GP2831

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND PATENT INTERFERENCES

Attorney Docket No. 040679/0439

19/Appeal Brief J. Hawkins 4-1-99

In re patent application of
Haruhiko MURATA et al.
Serial No. 08/825,400
Filed: March 28, 1997

Group Art Unit: 2831
Examiner: K. Cuneo

For: IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD HAVING SOLDER BUMPS

BRIEF ON APPEAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the provisions of 37 C.F.R. § 1.191-1.198, this is an Appeal Brief of the final rejection of claims 1-4 and 12, set forth in the final Office Action dated July 30, 1998. A Notice of Appeal was filed on January 29, 1999.

This Brief is being filed in triplicate, along with an appeal brief fee of $300.

REAL PARTY IN INTEREST

The real party in interest is the assignee of the application, NGK Spark Plug Co., Ltd.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-4 and 12 are currently pending in this application. The claims on appeal, 1-4 and 12, are set forth in Appendix A of the Appeal Brief.

STATUS OF AMENDMENTS

A Reply with amendments to the drawings After Final was filed on October 30, 1998. In the Advisory Action dated November 27, 1998, the Examiner indicated that the drawing amendments proposed in that reply would be entered upon filing of an appeal. An Examiner Interview was conducted on January 16, 1999.

SUMMARY OF INVENTION

The present invention relates to a circuit board with a substrate having a joining surface; and a plurality of solder bumps (solder balls, see specification page 1, line 7) disposed on the joining surface of the substrate in such a manner as to form a predetermined profiled line or surface pattern. As shown in Figure 2(b), the solder bumps have tops which are free, flat and leveled. The first feature of the invention is to provide flat solder bumps. As described in the specification, the flatness of the solder bumps assures proper connection between the solder bumps with the corresponding pads of a mating board.

The second feature of the invention is to provide leveled solder bumps. The levelness of the solder bumps makes the solder bumps co-planar, thereby compensating for any differences in the height of the respective mating pads, as shown by the dashed line in Figure 2(b). In particular, when a circuit board is curved or bent, the top portions of the different solder bumps lie in different planes, as shown in Figure 15(b). By leveling the top portion of the solder bumps, according to the present invention, solder bumps are provided in the same plane, thereby improving the reliability of the connections.

ISSUES

Whether claims 1 and 12 recite patentable subject matter under 35 U.S.C. § 102(e) and whether claims 2-4 recite patentable subject matter under 35 USC § 103(a).

GROUPING OF CLAIMS

Claims 1 and 12 are the independent claims at issue. For purposes of the rejections based on prior art, claims 1-4 and 12 stand or fall together.

ARGUMENT

The Rejection of Claims 1 and 12 under 35 U.S.C. § 102(e) and Claims 2-4 Under 35 U.S.C. § 103(a) Over Degani et al. (U.S. Patent No. 5,564,617) is Improper and Should Be Reversed.

In the final Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. § 102(e) and claims 2-4 under 35 U.S.C. § 103(a) as being unpatentable over Degani et al.

In the rejection, the Examiner relied upon Figures 3 and 5 of Degani et al. for rejecting the claims. Degani relates to a technique for assembling multichip modules. Figures 3 and 5 of Degani disclose a process for postioniong device chips on unreflowed solder paste patterns.

But Degani et al. does not teach or suggest the above-mentioned first and second features of the present invention. There is no mention in Degani about compensating for bent or curved circuit boards by levelling the top surfaces of solder bump, with the levelling feature recited in claim 1 of the subject application (see Figure 2b). Also, there is no mention in Degani to provide a flat top-surface of the solder bumps to assure a reliable connection. Finally, Degani does not even disclose solder bumps or solder balls. Degani uses a solder paste pattern which differs in material from solder bumps (balls) and in its reaction when heated to melt. In other words, the solder paste patterns 36 (see Figure 3) do not correspond to the solder bumps of the present application. Instead, the solder paste patterns are simply masses of solder paste.

In this regard, a telephone interview was conducted with the Examiner on January 16, 1999. In the Examiner Interview Summary sheet, the Examiner stated in pertinent part "Applicant suggested to change "solder bumps" to "solder balls." Actual determination cannot be made until the final form of the claims are reviewed, but this change appears to overcome the Degani et al. reference considering elements (36)." (Emphasis Added)

Applicant appreciates the Examiner's indication that "solder balls" are different from elements 36 (solder paste pattern) of Degani. Please note that the words "bumps" and "balls" are used interchangeably in the specification. Thus, the solder bumps as recited in claim 1 should be considered to be patentable over Degani.

Therefore, claim 1 (and 12) are patentably distinguishable from Degani. Claims 2-4 are also patentably distinguishable from Degani by virtue of their dependence from claim 1, as well as their additional recitations.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the final rejection of claims 1-4 and 12 should be reversed, and such reversal is respectfully requested.

Respectfully submitted,

3/29/99
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Appendix A

1. A circuit board comprising:

a substrate having a joining surface; and

a plurality of solder bumps disposed on said joining surface of said substrate in such a manner as to form a predetermined profile line or surface pattern;

wherein said solder bumps have tops which are free, flat and leveled.

2. A circuit board according to claim 1, further comprising circular pads interposed between said solder bumps and said substrate to serve as base layers of said solder bumps.

3. A circuit board according to claim 2, wherein said tops of said solder bumps have circular flat surfaces which are smaller in diameter than said pads.

4. A circuit board according to claim 3, wherein said tops of said solder bumps have nearly circular flat surfaces which are substantially equal in diameter to said pads, and the height of said solder bumps is smaller than the diameter of said pads.

12. A circuit board comprising:

a substrate having a joining surface; and

a plurality of solder bumps disposed on said joining surface of said substrate in such a manner as to form a predetermined profiled line or surface pattern;

wherein said solder bumps have tops which are unconnected, flat and leveled.